

Sputnik SpartanIle FPGA Development Board

User's Guide

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Introduction

The Sputnik SpartanIIE FPGA Development Board is a low-cost, flexible environment for both learning the basics of FPGA design and for developing complex system solutions. System I/O can be simulated with on-board switches, buttons, and LED's. Custom circuitry can also be interfaced via the two expansion headers.

This board can be ordered with various sizes of the SpartanIIE FPGA. The table below lists the size of devices available.

SpartanIIE Gate Density	Part Number
100K	33-BRD-0000006-01
200K	33-BRD-0000006-02
300K	33-BRD-0000006-03

Table 1 – Part Numbers of FPGA Variations

Circuit Description

The circuit is illustrated in Figure 1 (below):

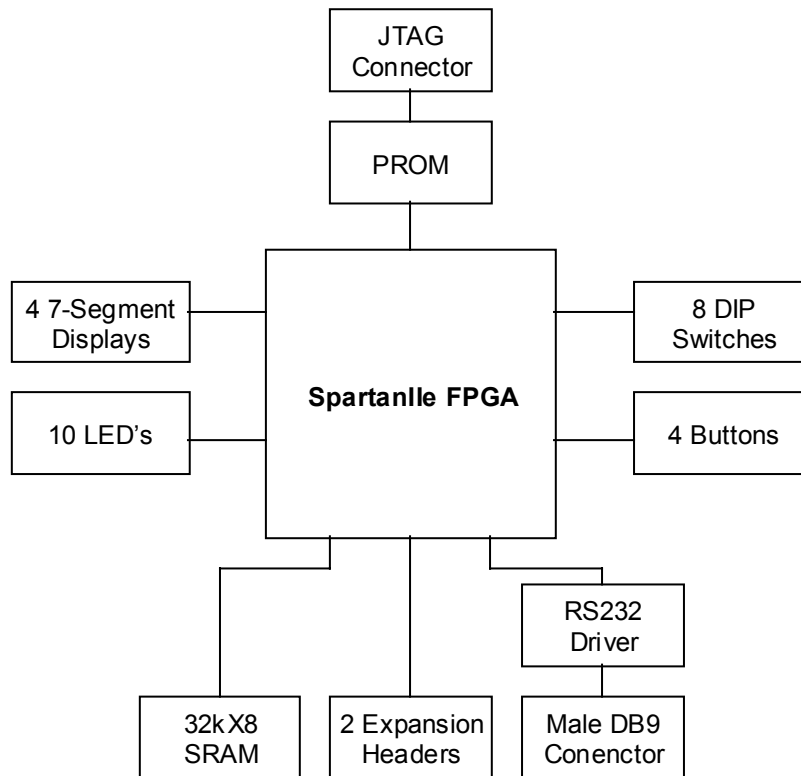


Figure 1 – Circuit Diagram

Input Power

Power is supplied to the board through the connector J4. This connector is “center-positive” i.e. the center 2.1mm pin provides power while the case of the plug provides ground. In case of error a reverse-voltage protection diode prevents circuit damage.

An external power supply must provide V_{IN} such that

$$4.0V \leq V_{IN} \leq 5.5V$$

Most designs will consume around 500mA. For very complex designs or designs in the larger FPGA sizes more current may be necessary. The [Xilinx Power Budget Spreadsheet](#) is discussed in [Xilinx Application Note 152](#). Use these resources to estimate the power requirements of a given design.

Xilinx SpartanIIe FPGA

The heart of this board is the Xilinx SpartanIIe FPGA. The footprint provided is a 208-pin PQFP. See Table 1 (above) for FPGA the device densities available.

See support.xilinx.com for the latest data sheets and more information about the SpartanIIe FPGA family.

Board I/O

This circuit provides a vast array of I/O connected to the FPGA:

- 4 tactile switches
- 8 DIP switches
- 4 7-segment displays (with left decimal point)
- 10 individual LED's
- 2 expansion headers with 12 i/o signals each
- one RS232 serial port

There are 12 signals available in each expansion header. These ports are designed to use high-speed signals. Each signal wire is between two ground conductors in the connected ribbon cable. This minimises cross-talk between adjacent signals and provides a return path for any signals traveling down the cable. Minimise the length of the connecting ribbon cable.

Memory

In addition to the block RAM that embedded in the FPGA, an external 32kx8 SRAM is also connected to the FPGA to provide additional external memory resources. This is a standard SRAM device and is completely controlled from the FPGA.

The SRAM device used is Cypress CY7C199. Consult the [data sheet](#) for the timing specifications and other design issues.

Using the Board

Programming the FPGA

The SpartanIIE is an SRAM based FPGA. These SRAM fuses are cleared during every power cycle and must be programmed. They can also be reprogrammed at any time.

One method is to program the devices directly from the DB25 JTAG Connector (J5). At the time of release the Xilinx ICE programming software Impact will not verify the SpartanIIE devices when programming directly. The software will recognise the device as a Vertex part but this warning can be ignored. Simply assign the bit file for the Spartan IIE design. In order to program the device successfully the “Verify” check box must be deselected. The FPGA should program but it is not possible to verify from Impact that the design has been downloaded correctly. The design will be active as long as power is maintained to the board. Once the power is removed the design will be cleared from the FPGA.

Another method is to use the onboard non-volatile PROM. On board power-up the FPGA will automatically load its design from the PROM. The PROM can be programmed using the DB25 JTAG Connector as well. This device programs correctly and reliably (with the verify option) from the Xilinx ICE programming software (impact.exe). This is the recommended method to program the FPGA. Note that the power must be cycled for the design to be loaded from the PROM to the FPGA.

Board Diagnostics

Included on the web page <http://www.stratforddigital.ca/products/sputnik> is a project containing a diagnostic firmware project. This is often useful during debugging when questions arise if the board is behaving as expected. This can be used to ensure that the hardware has not been damaged.

In order to test the Expansion Headers a loopback cable must be connected. It is simple to construct one with 1 foot of 26-conductor ribbon cable and two IDC 2x13 female connectors. This cable should have a straight-through pinout (i.e., pin 1 to pin 1, pin 2 to pin2, ...).

Use the .mcs file to program the PROM and cycle the power to load the PROM.

When programming is complete turn the power off and add the Expansion Header LoopBack Cable. Also connect a straight-through serial port cable (i.e. **not** a NULL modem cable) to a standard RS232 serial port. Configure the terminal with the settings in Table 2 (below):

Bits	8
Parity	No
Stop Bit	1
Baud Rate	115200
Flow Control	None

Table 2 – Diagnostic Serial Port Settings

Now turn on the board and the diagnostic test results will be printed on the terminal window. This will confirm if the hardware is still functional.

Design Resources

Latest information about the Sputnik FPGA Development Board is available at www.stratforddigital.ca/products/sputnik.

The Support section at support.xilinx.com contains a lot of design information and all the latest data sheets for the Xilinx SpartanIle and PROM's.

There is a growing collection of public domain IP modules at www.freecores.org. Most of these are implemented in VHDL or Verilog and can be implemented in the SpartanIle FPGA. If the original target of an IP module is for an ASIC or another FPGA family it may be necessary to optimise the design for the SpartanIle family.