

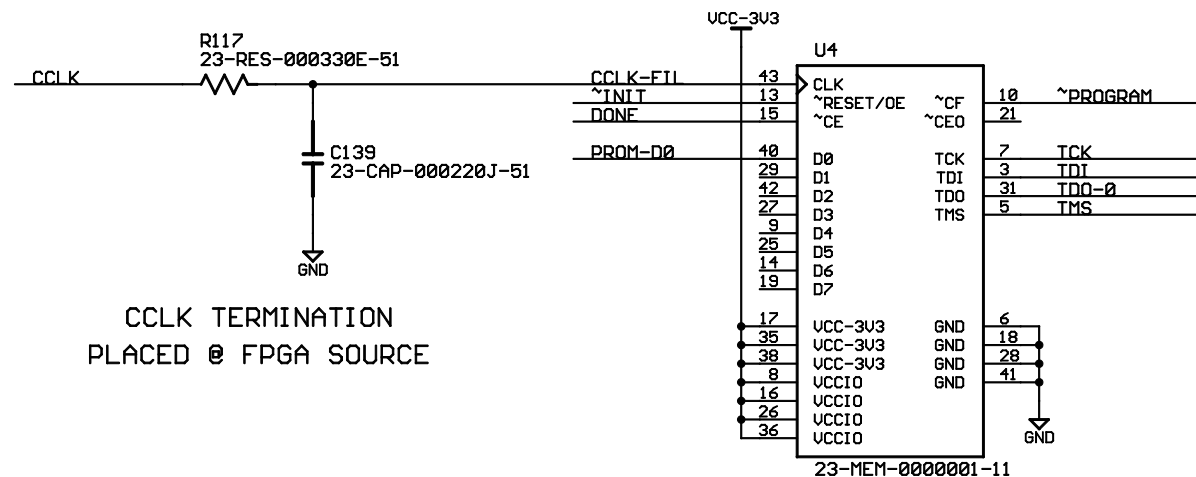
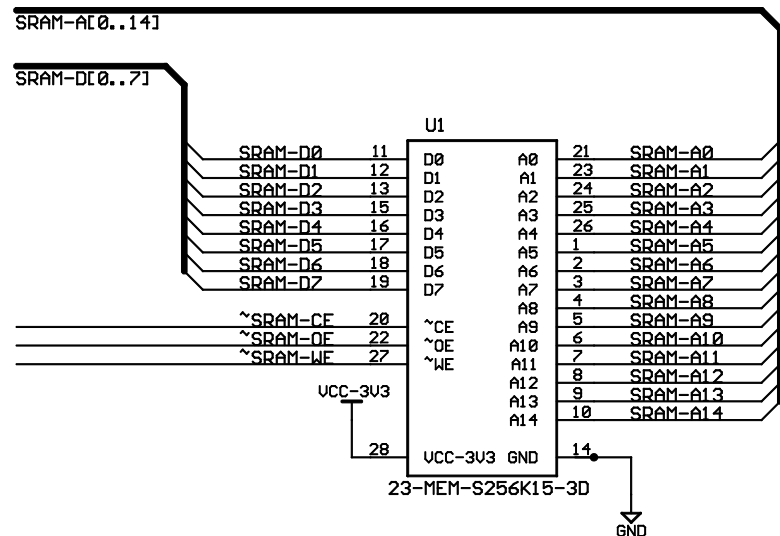
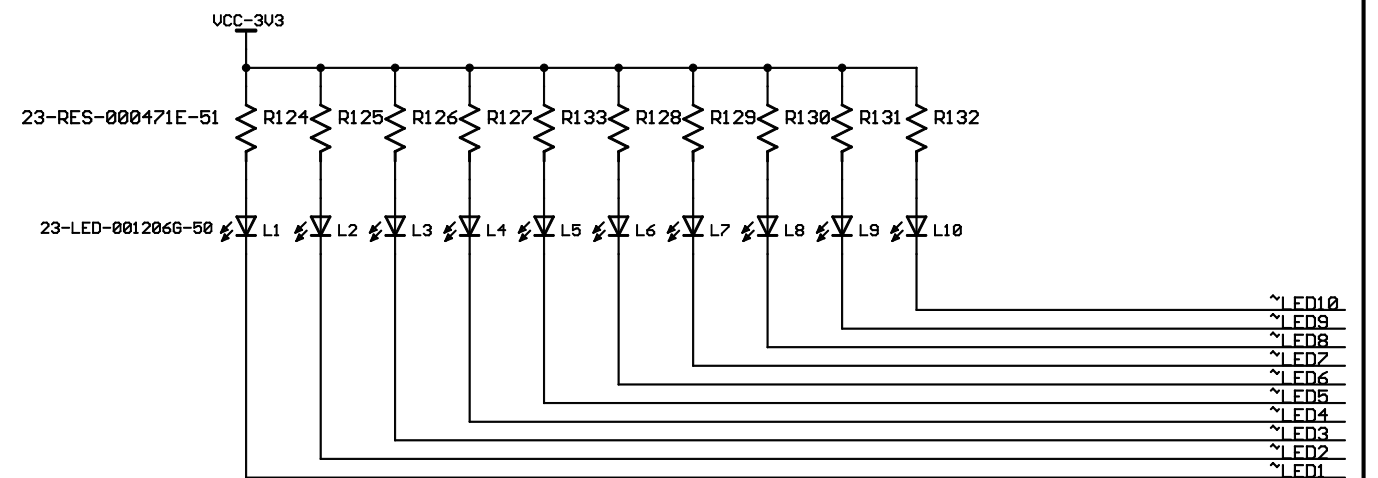
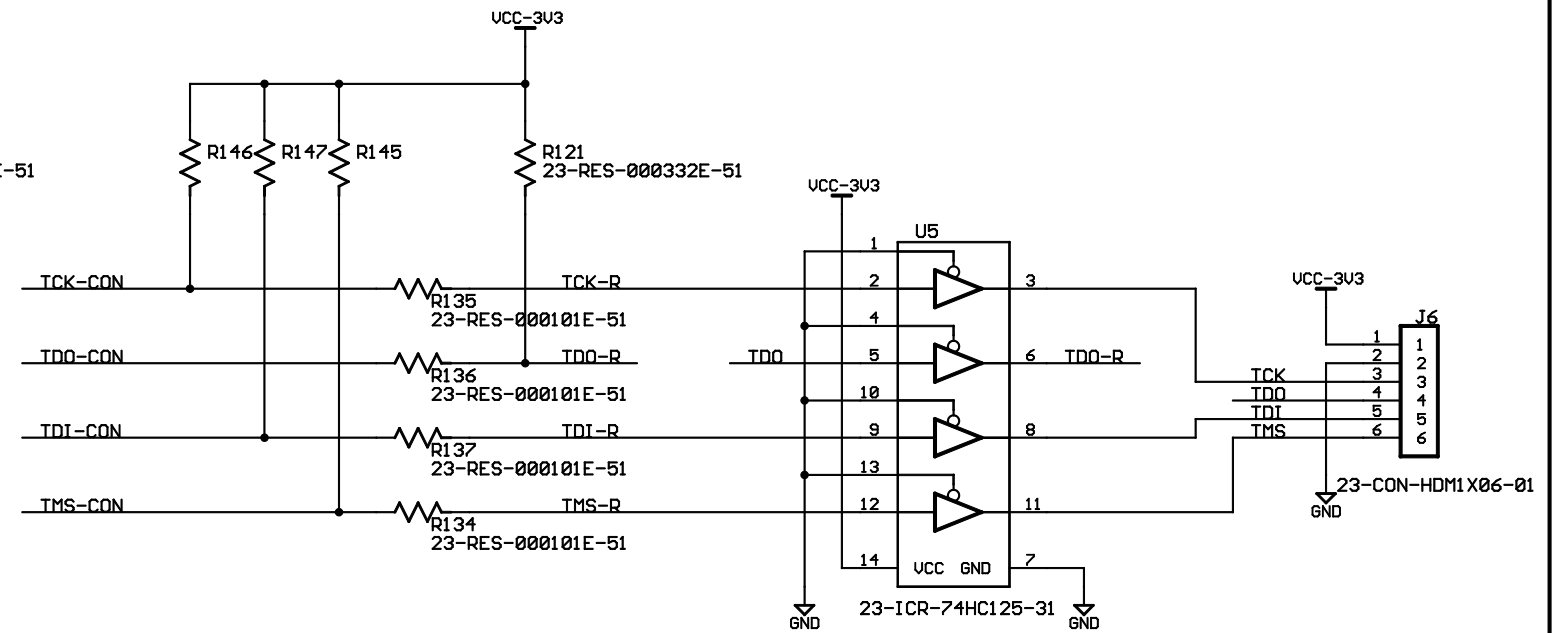
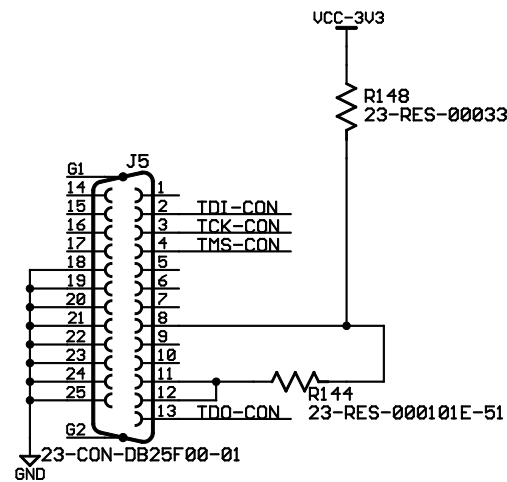
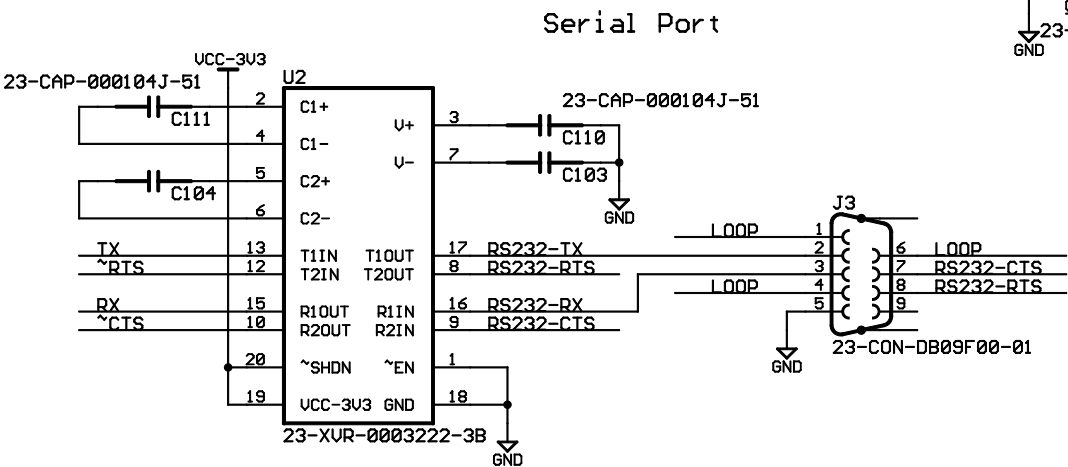
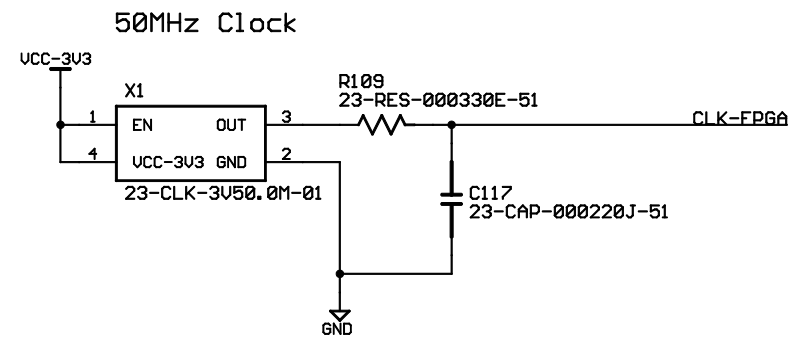
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**SpartanIIe
Development Board**

Schematic: SCH-33-BRD-000006-01-Rev1

Filename: SCH-33-BRD-000006-01
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CCLK TERMINATION
PLACED @ FPGA SOURCE

Populate resistor if PROM not populated



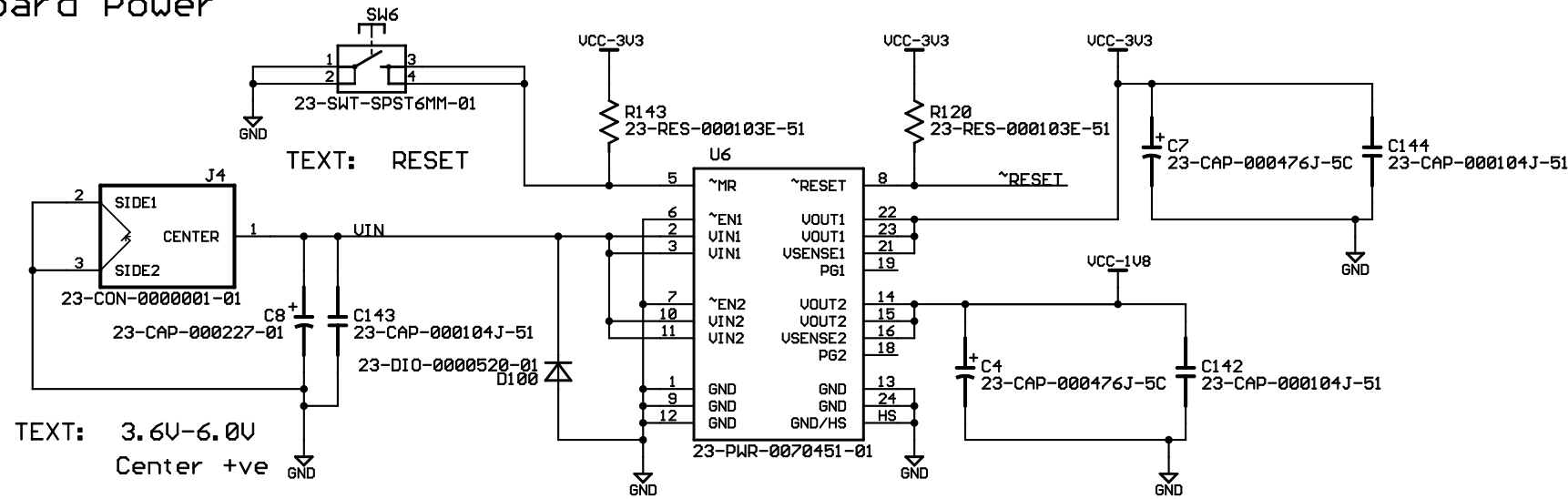
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Development Board

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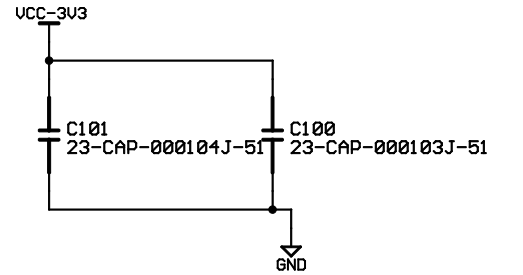
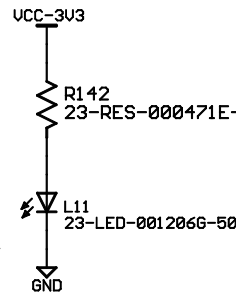
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Board Power

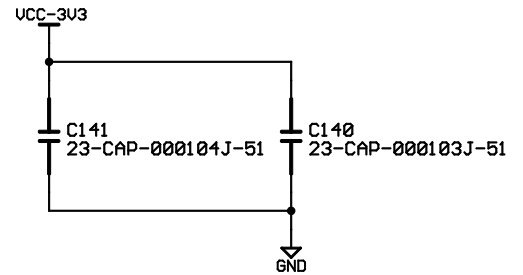


TEXT: 3.6V-6.0V
Center +ve

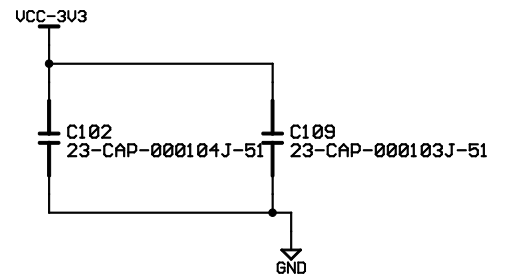
SRAM Decoupling



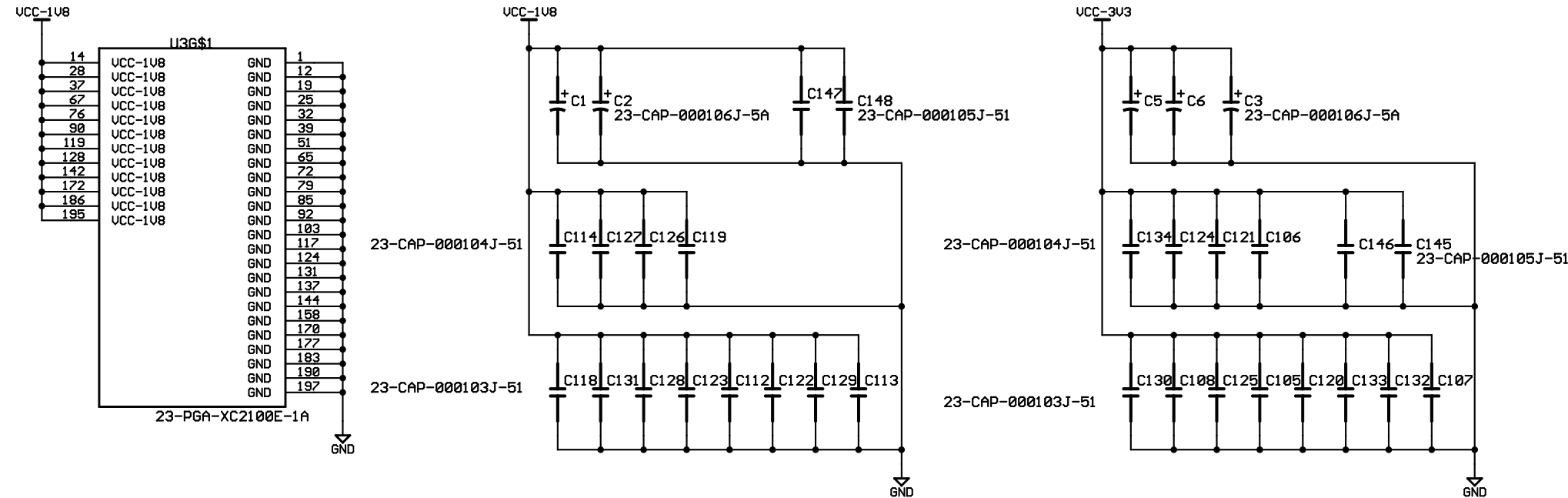
Buffer Decoupling



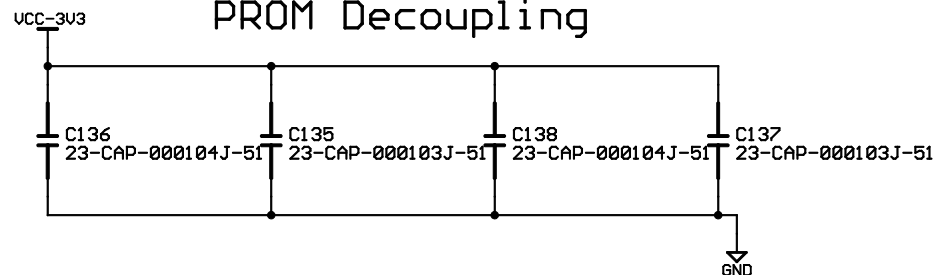
RS232 Decoupling



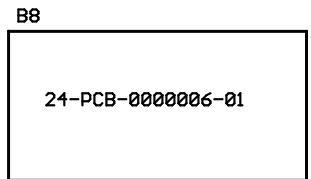
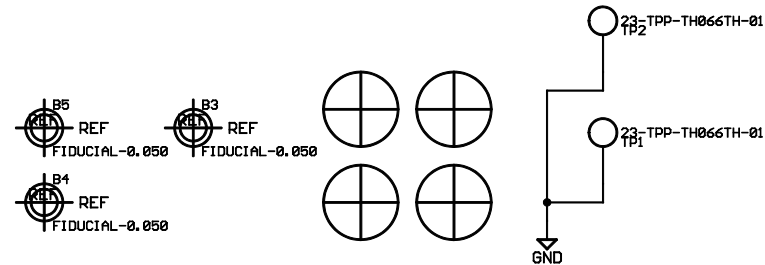
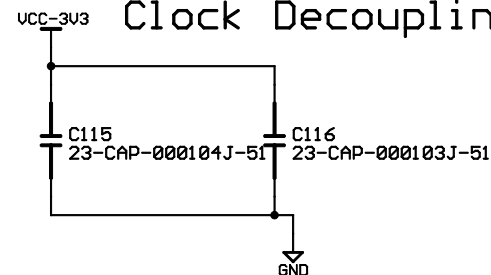
FPGA Decoupling



PROM Decoupling



Clock Decoupling



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Development Board**

Schematic: SCH-33-BRD-000006-01-Rev1

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