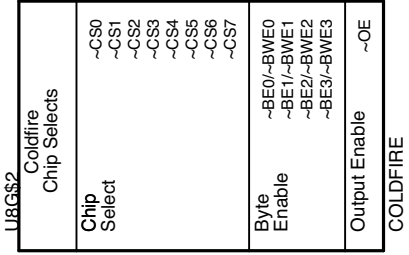
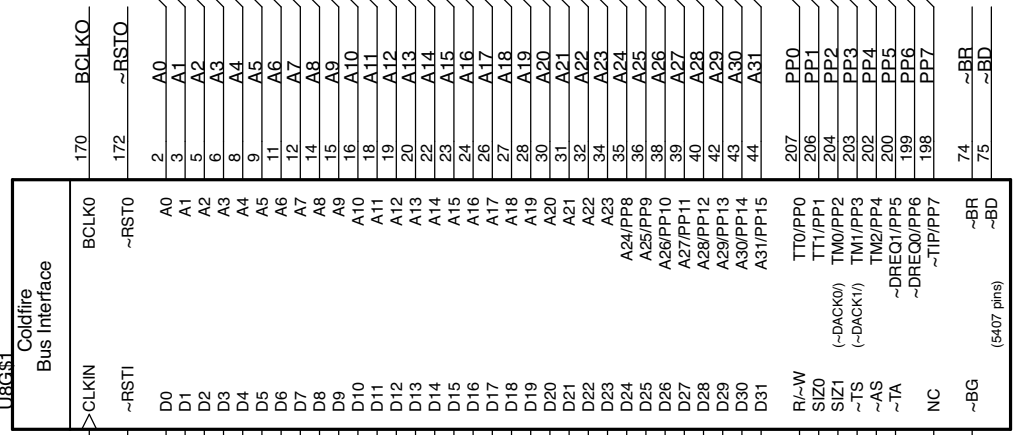
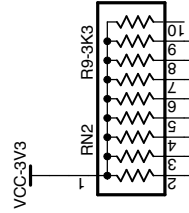
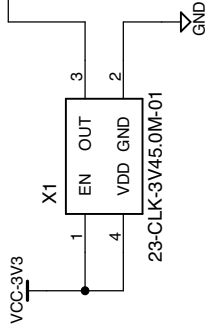


| | |
|---|----------------------------|
| CJ Design Services | |
| 5307/5407 Coldfire Development Board | |
| Block Diagram | |
| Schematic: | SCH-33-BRD-0000001-01-RevC |
| Filename: | janus |
| Page: | 1/13 |
| Timestamp: | not saved! |

A[0..31]
D[0..31]



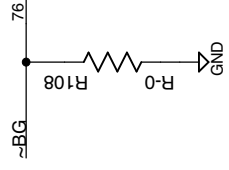
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Coldfire Main

Schematic: SCH-33-BRD-0000001-01-RevC

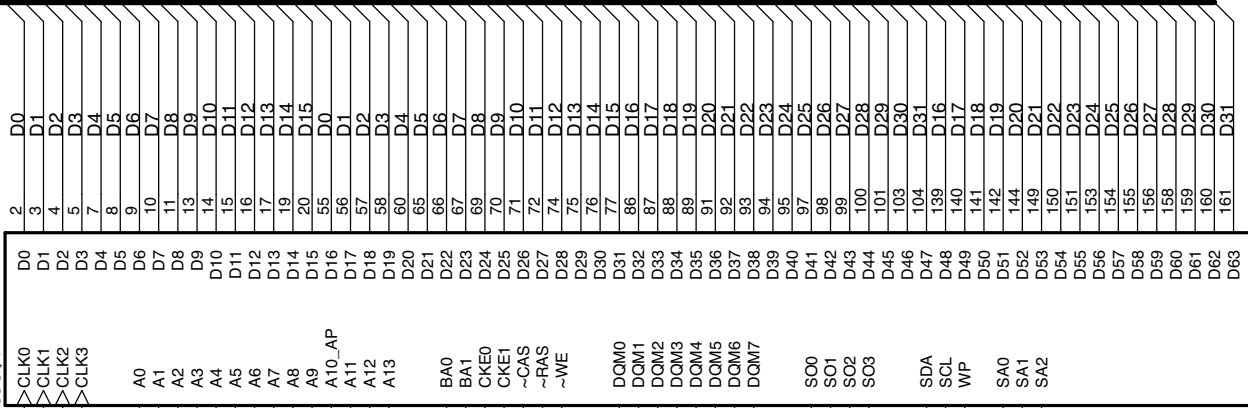
Filename: janus
Page: 2/13
Timestamp: not saved!



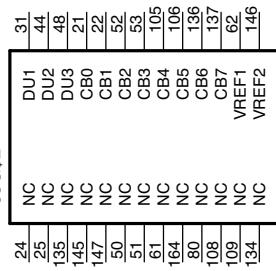
PP[0..7]

D[0..31]

J3G\$1

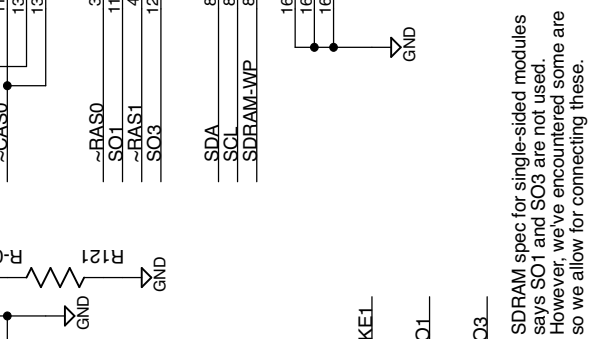
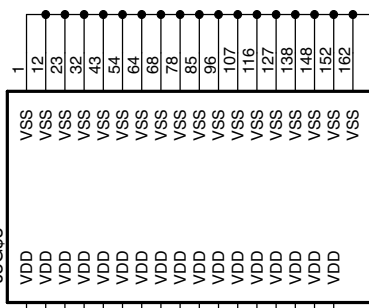


J3G\$2



VCC-3V3

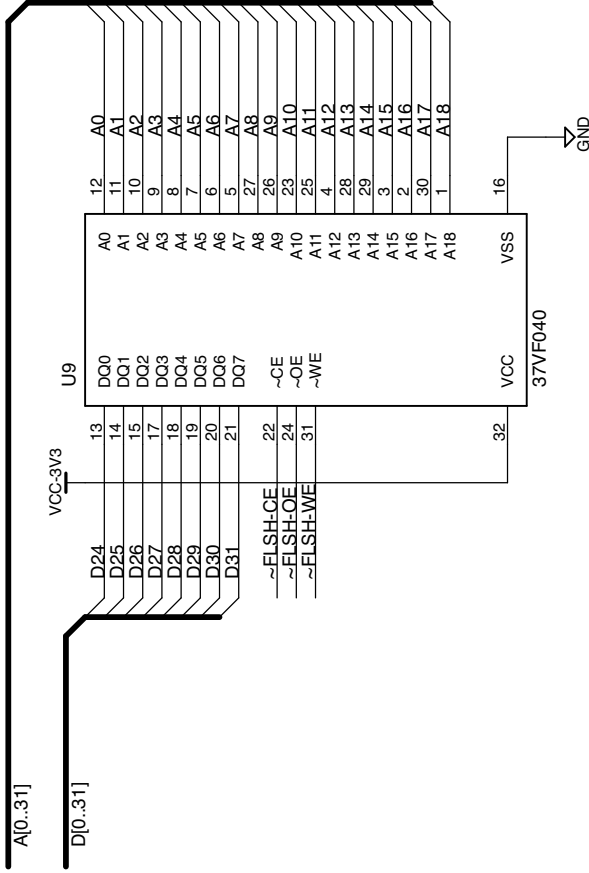
J3G\$3



SDRAM spec for single-sided modules says SO1 and SO3 are not used. However, we've encountered some are so we allow for connecting these.

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Development Board
SDRAM Memory

Schematic: SCH-33-BRD-0000001-01-RevC
Filename: janus
Page: 5/13
Timestamp: not saved!



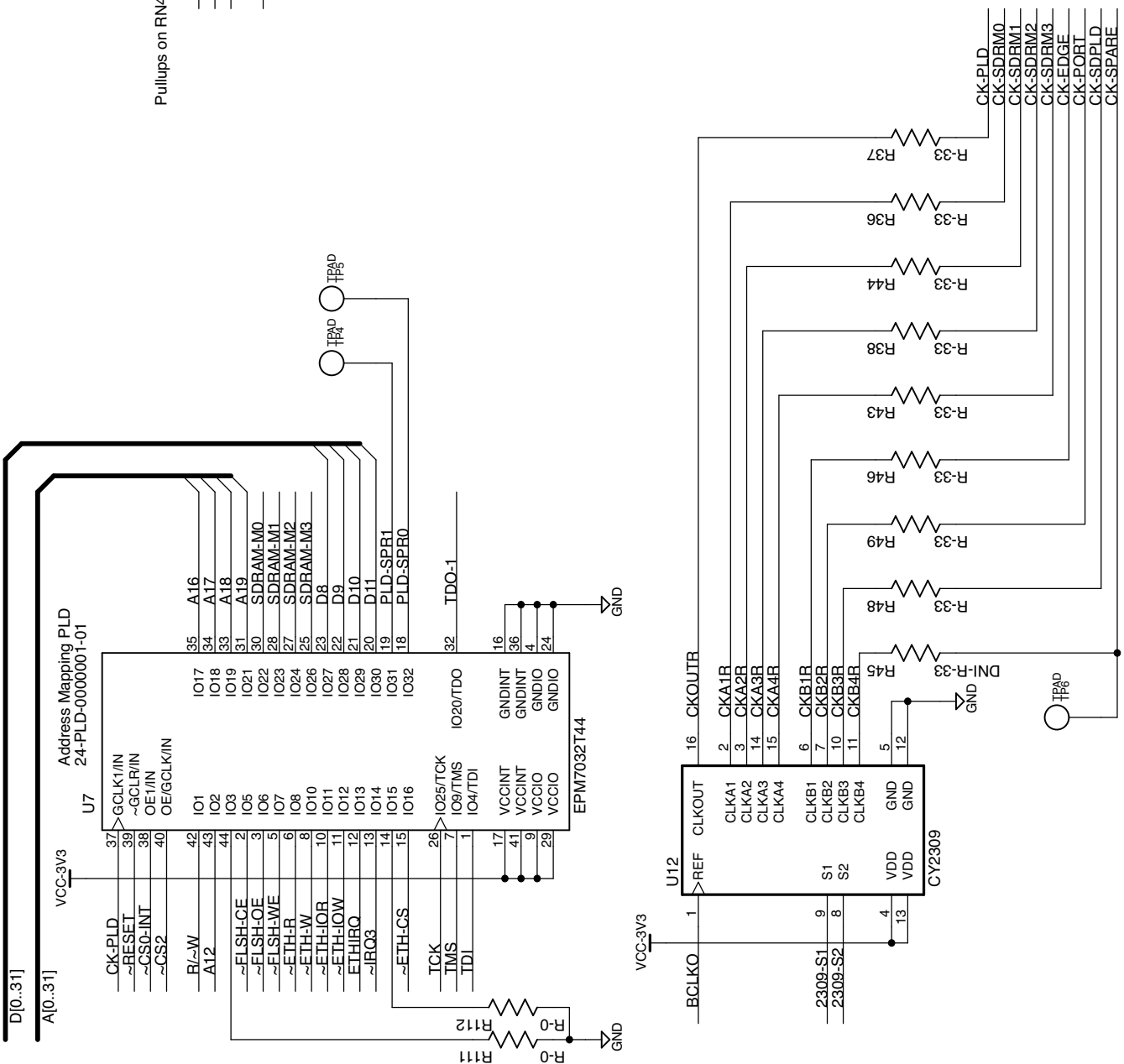
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Non-Volatile Memory

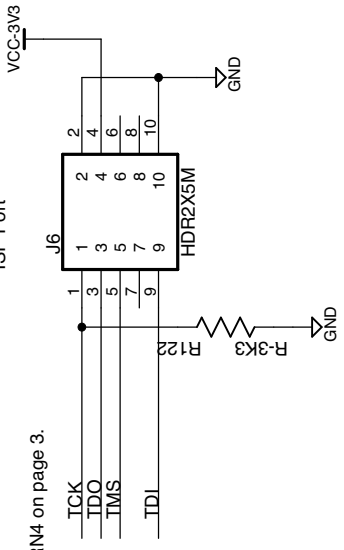
Schematic: SCH-33-BRD-0000001-01-RevC

Filename: janus
 Page: 6/13
 Timestamp: not saved!



Board Text:

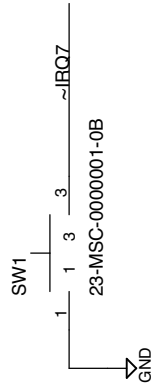
ISP Port



Pullups on RN4 on page 3.

Board Text:

Soft Reset



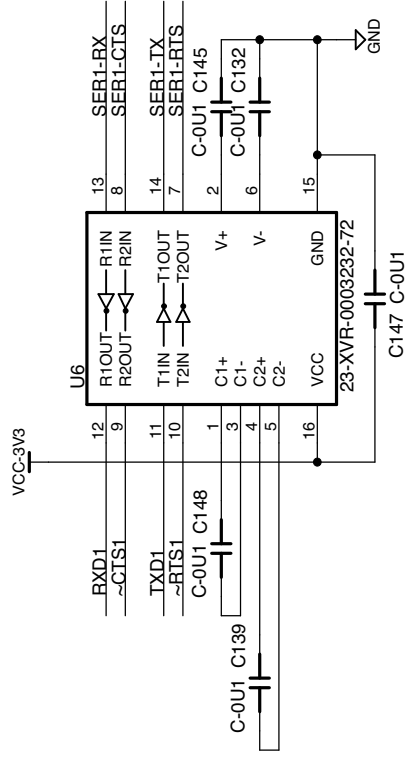
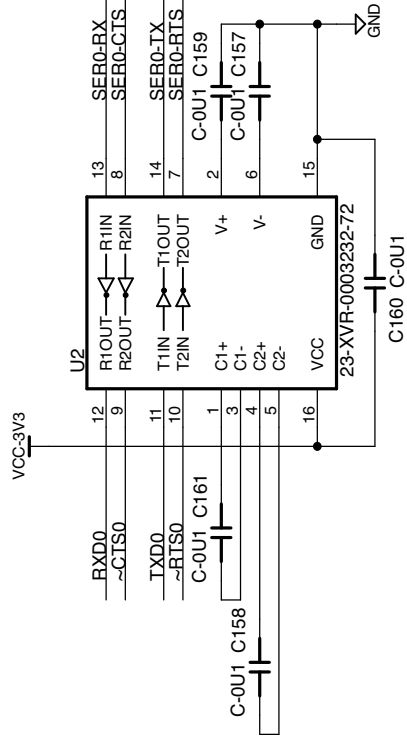
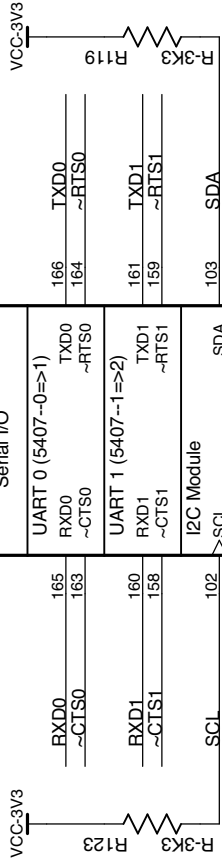
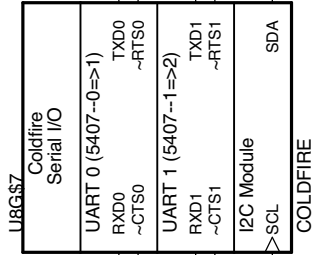
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**5307/5407 Coldfire
Development Board**

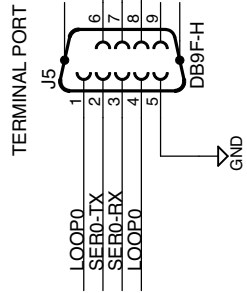
System Resources

Schematic: SCH-33-BRD-0000001-01-RevC

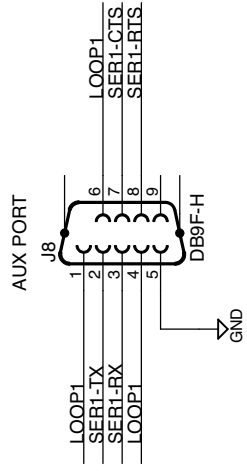
Filename: janus
Page: 7/13
Timestamp: not saved!



Board Text:



Board Text:



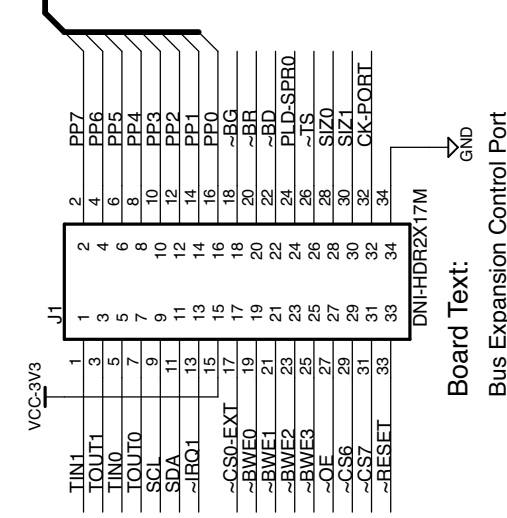
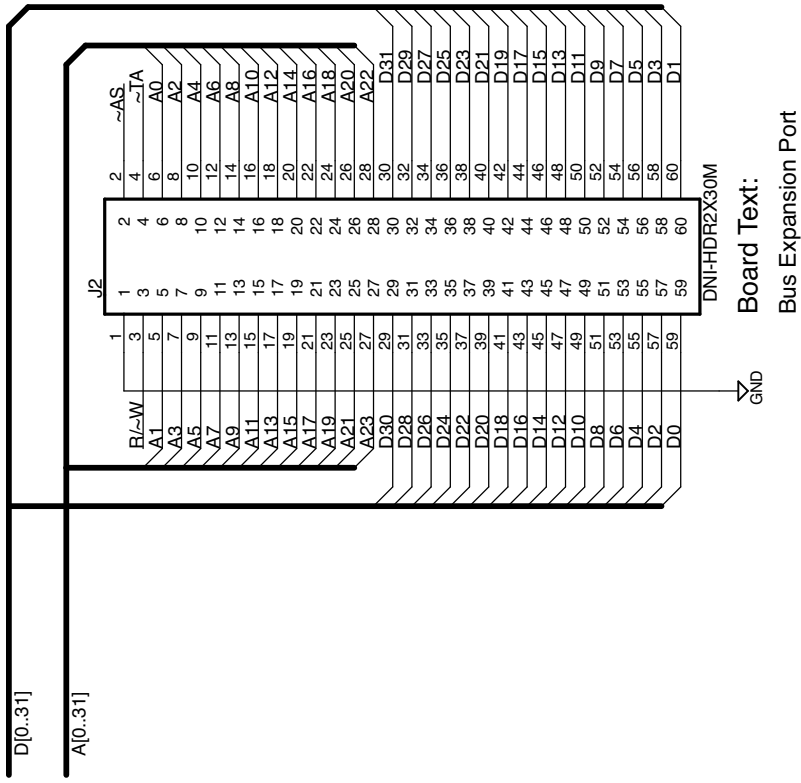
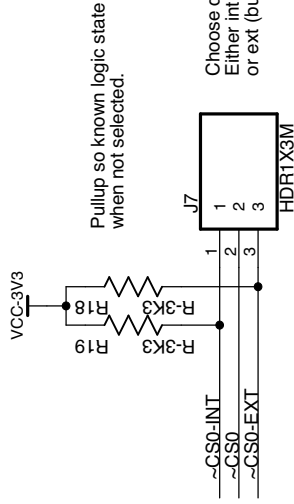
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RS232 Serial Ports

Schematic: SCH-33-BRD-0000001-01-RevC

Filename: janus
 Page: 8/13
 Timestamp: not saved!



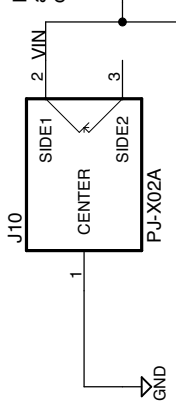
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Bus Expansion Port

Schematic: SCH-33-BRD-0000001-01-RevC

Filename: janus
Page: 9/13
Timestamp: not saved!



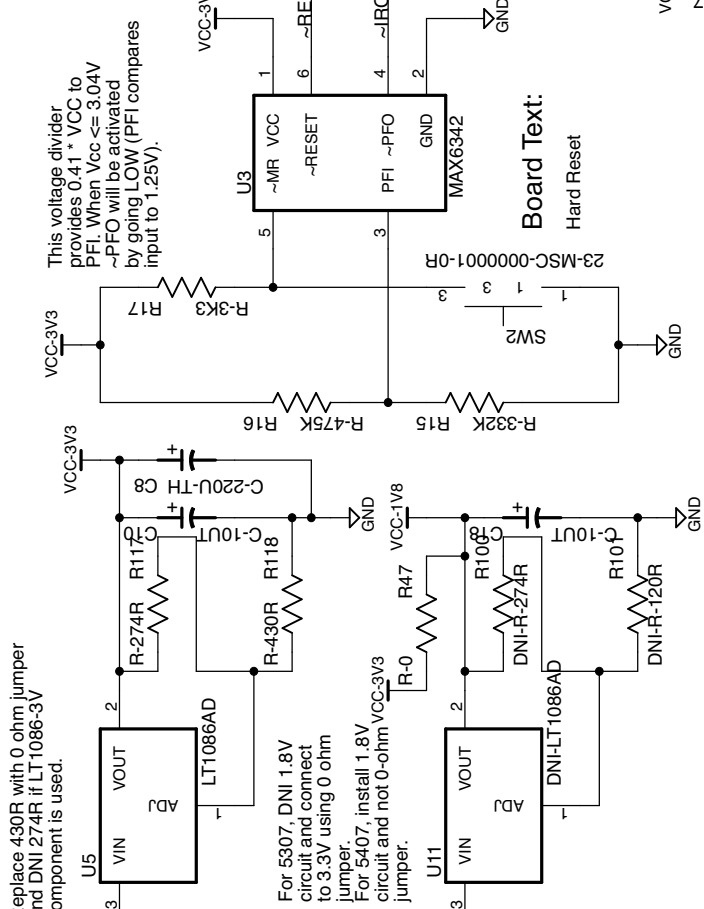
SIDE 2 connected to SIDE 1 when connector NOT inserted.

Board Text:

6-12VDC Center GND

Decoupling Cap Table

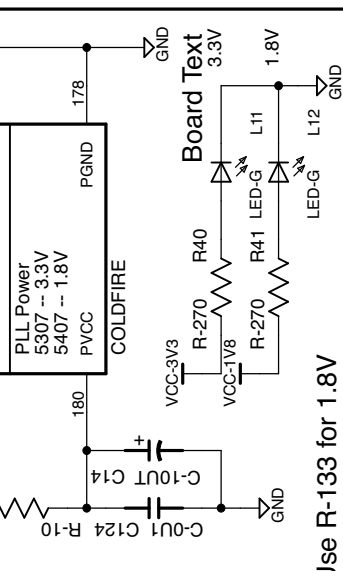
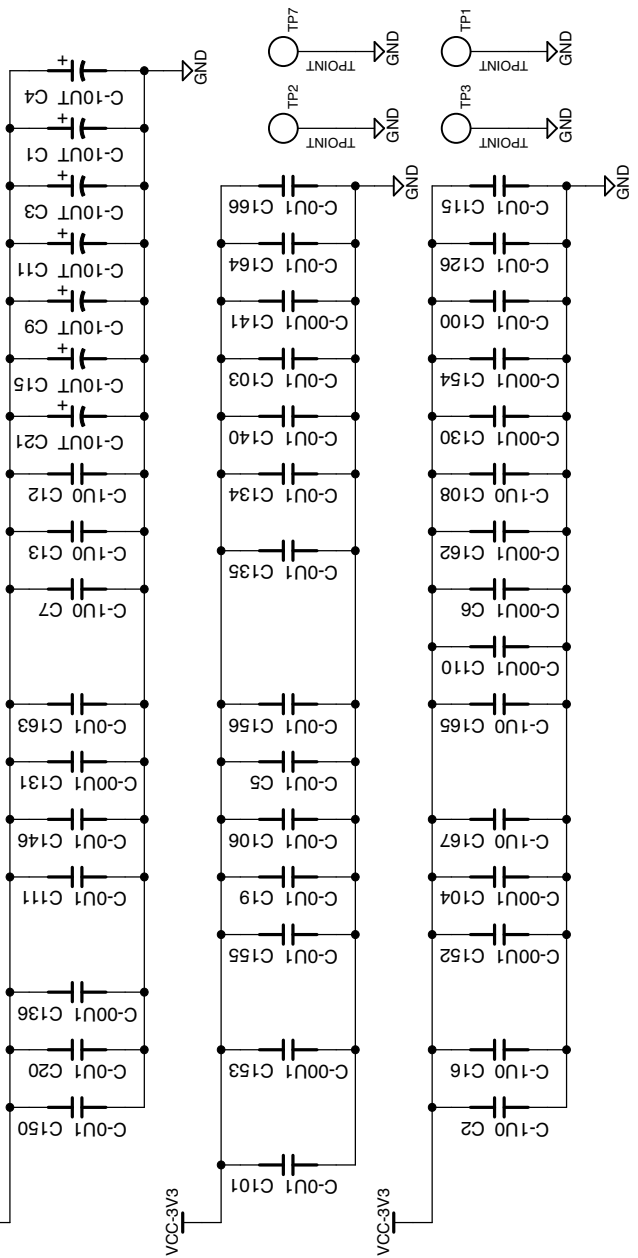
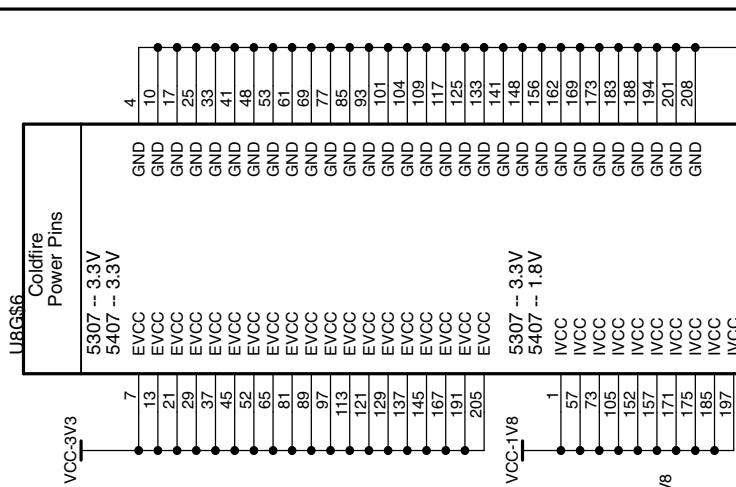
| Component | 0.01 | 0.1 | 1.0 |
|---------------|------|-----|-----|
| ColdFire | 7 | 15 | 6 |
| CS8900A | 2 | 3 | |
| OSC-40M | 1 | | |
| CY2309 | | 3 | |
| 16244 | | 2 | |
| 93LC46 | | 1 | |
| SDRAM MUX PLD | 2 | 2 | |
| ADD MAP PLD | 2 | 2 | |
| 28LV256 | | 1 | |
| 37VF020 | | 2 | 10T |
| General | | 4 | 4 |



Board Text:

Hard Reset

This voltage divider provides 0.41 * VCC to PFI. When Vcc <= 3.04V ~PFO will be activated by going LOW (PFI compares input to 1.25V).



Use R-133 for 1.8V

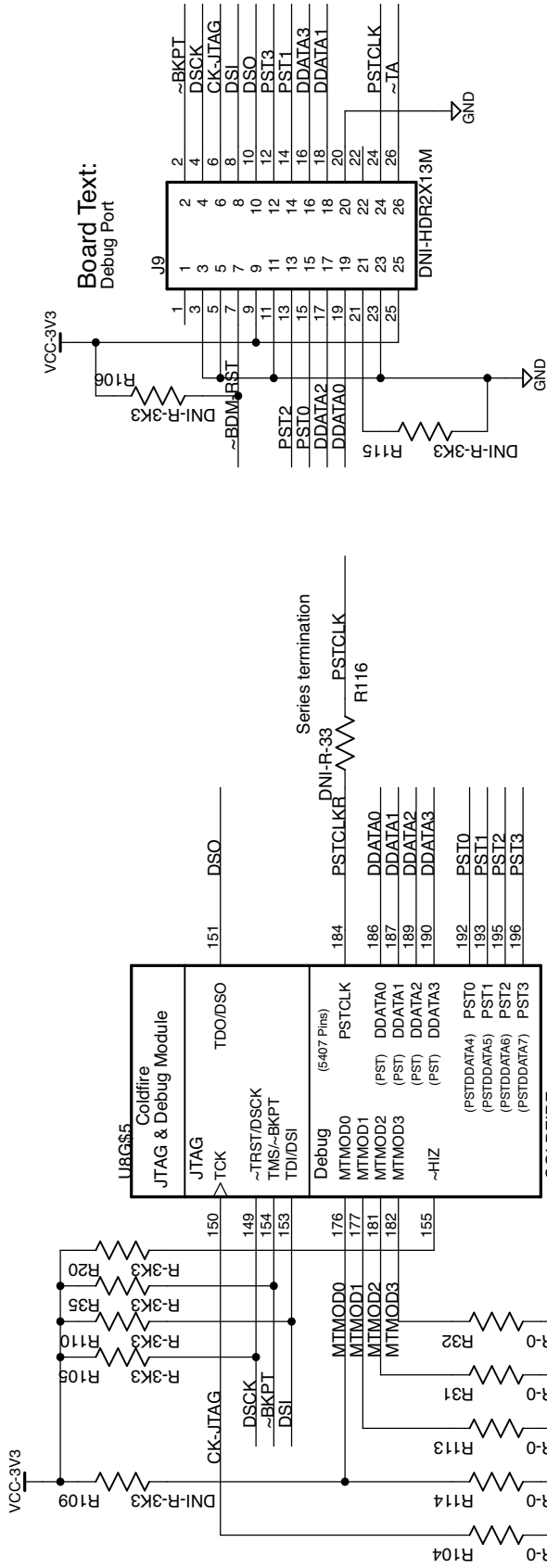
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5307/5407 Coldfire Development Board

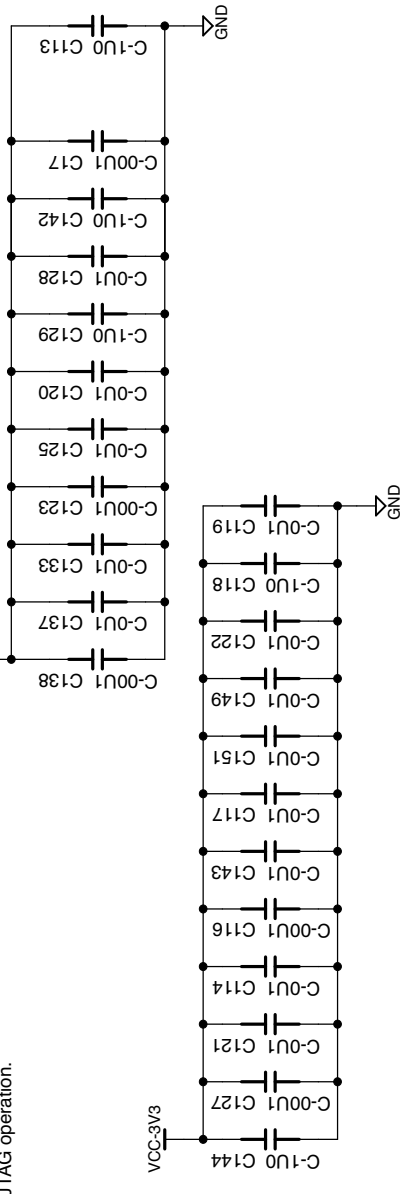
Power and Termination

Schematic: SCH-33-BRD-0000001-01-RevC

Filename: janus
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Timestamp: not saved!



Hardwired for normal operation.
Remove pull-down resistor on mtmod0
and install pullup resistor for
JTAG operation.



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5307/5407 Coldfire Development Board

Debug Port

Schematic: SCH-33-BRD-0000001-01-RevC

Filename: janus
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Timestamp: not saved!

| Revision | Description |
|----------|--|
| RevA | Initial prototype board. |
| RevB | Corrected signals going through SDRAM connector non-plated holes. |
| RevC | Many corrections. See CVS log files. |
| RevD | Added 4 feducials and reduced mounting holes to 0.125" for board stuffing. |

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**5307/5407 Coldfire
Development Board**
Revisions

Schematic: SCH-33-BRD-0000001-01-RevC

Filename: janus

Page: 13/13

Timestamp: not saved!